**Single phase clock distribution using VLSI technology for low power**

**Abstract**

The clock distribution network consumes nearly 70% of the total power consumed by the Ie since this is the only signal which has the highest switching activity. Normally for a multi clock domain network we develop a multiple PLL to cater the need, this project aim for developing a low power single clock multiband network

which will supply for the multi clock domain network. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are proposed based on pulse-swallow topology and the designed is modeled using Verilog simulated using Modelsim and implemented in Xilinx.

**Tools:**

* Modelsim simulator
* Xilinx synthesis

**Language:**

* Verilog HDL